Advanced Packaging

Next-generation Electronics Packaging Using Flip Chip Technology

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There is a rapid increase in the number of electronic packages using flip chip technology. With the ongoing expansion of the Internet, mobile phones, PDAs, desktop computers and laptops, digital camcorders, digital cameras and other electronic-based consumer products, the flip chip revolution is in full swing. Product functionality has never been more demanding, and time-to-market and volume production are more critical than ever. Flip chip packages now exist for a range of products from few lead RFIDs to more than 2,000 lead BGAs. Substrate technology has moved from traditional ceramics to a wide range of organic materials, enabling a multitude of different package applications built around flip chip technology.

This increased use of flip chip technology is driving the need for the next generation of production equipment, including flip chip bonders and underfill dispensers. These flip chip machines require many advanced features to satisfy new manufacturing requirements and minimize the cost of ownership of integrated device manufacturers and subcontract manufacturers.

Inherent Advantages of Flip Chip Technology

A key advantage of flip chip technology is size. Flip chip packages do not require peripheral space for the wire bonds. They can be made smaller than wire bond packages with a similar I/O count. For die with a high I/O count, flip chip technology offers large space savings because the I/O can be arranged in an array on both die and substrate. This eliminates the need for traces to the chip edge from internal interconnect points. At the substrate level, routings can be directed through multiple internal layers. This array architecture can be used to achieve space savings, similar to the savings between BGA and QFP. Overall material cost (package and die), when taking into account die shrinkage enabled by flip chip, is less. Flip chip technology also offers the potential for lower total package height, since no extra clearance is required for wire bonds or encapsulation/mold compound above the die. The space savings of flip chip technology translate into a geometry that delivers the solution for today's high I/O consumer end-products, such as digital video cameras.

Another key advantage is improved performance. A short signal path provides for low inductance, resistance and capacitance, the result being a faster signal and better high frequency characteristics. Flip chip technology provides improved functionality in terms of an increased number of I/Os, plus the concentration of more signal, ground and power connections in a smaller area. The technology offers better thermal capabilities, since an external heat sink can be directly added above the chip to remove heat.

Solder reflow flip chip has fewer process steps compared to traditional epoxy die attach and wire bonding. Operations such as wire bonding and encapsulation or molding are eliminated. Flip chip technology integrates all the package assembly steps in one operation. Assembly time, total number of process steps, overall capital equipment costs, the number of pieces of equipment, as well as other factors result in a reduced cost of ownership.

Flip Chip Package Types

There are three basic types of flip chip packages:

THE FLIP CHIP REVOLUTION IS IN FULL SWING

Illustration by Gregor Bernard

Figure 1. Die flipping mechanism

Figure 2. Flux dipping

FC-BGA and High-performance FC-BGA (HFC-BGA). These two packages cater to I/Os of 100 to more than 1,500, with BT laminate or sophisticated multilayer substrates. The HFC-BGA is thermally enhanced by the attachment of a metal heat sink that can effectively remove the heat and improve thermal characteristics.

Ceramic FC-BGA/PGA. This ceramic package provides better heat dissipation for high thermal conductivity and a coefficient of thermal expansion more closely matched to silicon.

FC-CSP. This package offers chip-scale geometry for packages with less than 200 I/Os. This package provides better protection for the die than chip-on-board technology. It prevails over known good die in low-cost test and burn-in. It is intended to provide a thin, small profile and lightweight packaging. Applications include RFICs, and memory ICs.

Flip Chip Assembly Process

There are four primary types of flip chip attachment/assembly processes: solder reflow, gold stud bump, anisotropic conductive films and anisotropic conductive epoxy. For the purposes of this paper, flip chip die bonding are being addressed as relevant to the solder reflow method.

This paper focuses on two major steps: die bonding and underfill dispense.

The first step in the die bond process is to load substrates to the flip chip bonder. Substrates are unloaded from magazines and indexed into the flip chip bonder. High system speeds are possible when the substrate loading operation can be done in parallel with pick-and-place operations. The loader must be able to handle substrates in strip form (e.g., BGA strip), as well as singulated substrates in carrier boats. Carrier boats are loaded into magazines, and the magazines are placed in the loader. The carrier boats are then indexed into the flip chip bonder, one at a time.

Flip Chip Bonder

The flip chip die bonder is the piece of equipment responsible for picking the die from the wafer, flipping the die, dipping it into flux and placing it aligned on the substrate. First, the substrate strip or carrier is indexed into the work area and the substrates are locked in place with vacuum, using a vacuum chuck. Alternatively, mechanical clamping is sometimes used. It is important that the vacuum chuck have very good planarity relative to the die placement head. The vacuum chuck must be easy to exchange and set up to ensure rapid changeover. Vacuum sensing must ensure that the substrates are secured at all times to enable accurate placement. Alignment of the substrates using a down-facing camera is essential for accurate placement. The system determines the substrate coordinates by using substrate fiducials or alignment marks. Most systems today use pattern recognition, in addition to geometric feature recognition. Pixel size and vision repeatability are critical factors for accuracy. Quality optics and lighting, plus various light types and colors, play an important role and are used to obtain better definition.

Die Feeding

Next-generation flip chip bonders require 300-mm wafer capability. In this step, die is presented in wafer format with the bumps up. At this stage, wafers are fully tested and diced. Good die on the wafer are determined either via an ink dot scheme or from a wafer result map. Electronic wafer mapping is usually preferred over ink dot when processing flip chip die. 300-mm wafer handling includes the ability to dock an industry standard wafer cassette cart. The wafer is loaded from a wafer cassette, which can hold up to 25 wafers, onto the wafer table. During the loading process, the bar code located on the wafer frame is read and the correct wafer map file downloaded from the server. The wafer is stretched, in order to prevent die edge chipping, and the first good die is located using a wafer camera. The wafer table is indexed to the correct location for the flipper to pick and flip the die. The wafer map file (cyber wafer) is aligned to the wafer and the machine begins to pick good die.

Package type	Nr. I/O	Package size	Substrate type	Ball pitch
FC-CSP	36 ~ 200	7x7 ~ 15x15	Laminate	0.8/1.0
Ceramic FC – BGA/PGA	< 1421	27x27 ~ 50x50	Ceramic	0.8 ~ 1.27
FC-BGA	100 ~ 1521	11x11 ~ 40x40	Laminate	1.0/1.27
HFC-BGA	256 ~ 1521	27x27 ~ 40x40	Laminate	1.0/1.27

Table 1. Common flip chip packages

Die Flipping

The flipper will pick good die from the wafer with the bumps up, and flip it so that the bumps face down (Figure 1). This is done so that the flux head can repick the die in the flux-ready orientation. The flipper's initial movement after picking the die must be straight up, before translating into a rotational movement. This is to prevent the die from colliding with other die on the wafer.

The flipper pickup tool must not damage the bumps. It must have enough of a vacuum to hold the die securely during flipping. Flipper movement, speed and acceleration must be programmed and synchronized with the eject system and the bond head in order to prevent damage to the die and eliminate unnecessary delays.

Flux Dipping

In this process, the die is picked from the flipper by the bond head and dipped into flux (Figure 2). The flux delivery system presents an important opportunity to improve yields and throughputs. Fine control over the depth of flux is achievable with attention to the properties of the flux and to the mechanics of the delivery system. By programming the speeds of the plate action, throughput can be optimized while still attaining precise control over volume. The fluxer consists of a plate with a precision-machined flux well. The flux thickness is determined by the depth of the flux well and the surface tension of the fluxing fluid. A range of plates can be exchanged to achieve different thicknesses. Fluxer indexing speed should be programmed to account for different flux viscosities. Heating the flux can help achieve optimum bump wetting.

Fluxer planarity is essential to ensure good process control and prevent open joints, as the amount of flux on the bumps will directly influence bump reflow. The flux plate and flux reservoir must be easy to exchange and clean, without the need for special tools.

Flux dwell time must be programmed in accordance with the type of flux used and its particular wetting capabilities.

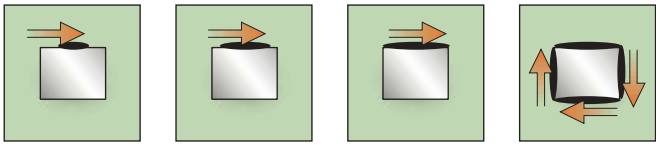

Figure 3. Typical underfill process

The amount of time spent fluxing the chip will directly influence system throughput. However, by performing the flux operation in parallel with other operations, such as picking from wafer and placing on the substrate, the flux step can be taken out of the critical path. The can dramatically increase the unit per hour rate (UPH) of the system by as much as 50 percent. Next-generation flip chip bonders must perform fluxing in parallel with the pick-and-place cycle to achieve competitive throughput rates.

Die Pick-and-place

The flux head picks the die from the flipper, from the non-bumped side, with the bumps facing down. The system bond head will pick the die from the flux for presentation to the upward-looking camera for vision alignment. The vision system determines the X-Y & θ offset from the die to the bond head. Based on this, the bond head position is adjusted to ensure that the die is placed accurately on the substrate. Lighting is a critical part of the vision process, since the fluxed bumps must be located accurately and fluxed bumps can be challenging to basic vision systems.

Bond head planarity to the substrate is a must for accurate placement. Small deviations can cause the die to shift during placement. Bond force control and bond force repeatability are very important in achieving accurate and repeatable placements. Closed-loop, controlled bond force will ensure highly accurate placements and repeatability, achieving a stable process and a high Cpk.

Once the substrates are populated with die, the carrier is either loaded back into a magazine or transported to a reflow oven. The offloading of carriers offers another opportunity for throughput gains. Improvement is realized if carriers can be exchanged quickly, in parallel with the pick-and-place cycle. Although a fast action, the indexing of carriers must be smooth to prevent die shifting. An excellent means of fast carrier exchange is to combine the carrier conveyor with a mechanical device. With this approach, the conveyor can be used to bring carriers to and from the system, but the faster mechanism can be used for rapid delivery of the carrier to the assembly area. By controlling acceleration and deceleration of the carrier mechanism motion, the fastest movements are possible without disturbing the placed die. Performing carrier exchange in parallel with the die pick-and-place cycle is especially important when the number of die per carrier is low.

Flip chip technology offers the potential for **lower total package height, since no extra clearance is required** for wire bonds or encapsulation/mold compound above the die.

Reflow Oven

The final stage of the flip chip die bonding assembly process is solder reflow. Solder bumps are reflowed in an oven with an inert atmosphere, creating a solder joint that also acts as the electrical interconnect. A typical reflow oven used in flip chip applications will have multiple heat zones and can reach temperatures of up to 400°C. The actual reflow profile is a function of belt speed (oven indexer) and heat zone temperature settings. Carriers with reflowed chips are either loaded back into a magazine or transported to a next step.

Underfill Dispensing

The second major step of the solder reflow flip chip assembly process is the dispensing of underfill. In this step, underfill material is dispensed alongside the die, and the material is drawn between the die and the substrate via capillary action. Underfill material is used to protect the interconnect area from moisture. It also reinforces the mechanical connection between the substrate and the die. Underfill compensates for any difference in the thermal coefficient of expansion between the chip and the substrate.[1]

The first step in the underfill process is to load substrates to the underfill dispense system. Substrates are loaded on carriers from magazines or the previous process and may pass through a plasma clean operation. Once the substrates are in place, epoxy base material is dispensed along one or two edges of the flip chip. Capillary action is initiated as the material

contacts the edge of the die, and even further enhanced as the material migrates from bump to bump underneath the die. Depending on the size of the package, several passes might be required to completely fill the area. Once the material has reached the side opposite from where depositing commenced, a fillet is typically dispensed around the remaining sides to complete the seal around the flip chip (Figure 3). Many enhancements have been made to underfill dispense systems to increase UPH. One approach is to use dual-lane processing. The dual lanes improve UPH by allowing the system to execute process steps on one lane, while the other is busy; for example, waiting for underfill material to flow or transferring parts in or out of the system (Figure 4). This feature can achieve double-digit improvements in machine efficiency.

The space savings of flip chip technology translate into a geometry that **delivers the solution for today's high I/O consumer end-products**, such as digital video cameras.

Substrate Preheating

Substrate temperature uniformity and quick ramp up are critical semiconductor packaging process parameters. Underfill dispense systems are configured with contact heating stages to elevate the temperature of the substrate before, during and after dispensing. Preheating occurs before the carrier reaches the dispense station. Heating the substrate before dispensing is required to enhance material flow during dispense, which increases throughput. An additional benefit of preheating is that the moisture content of the package is reduced, which improves reliability.

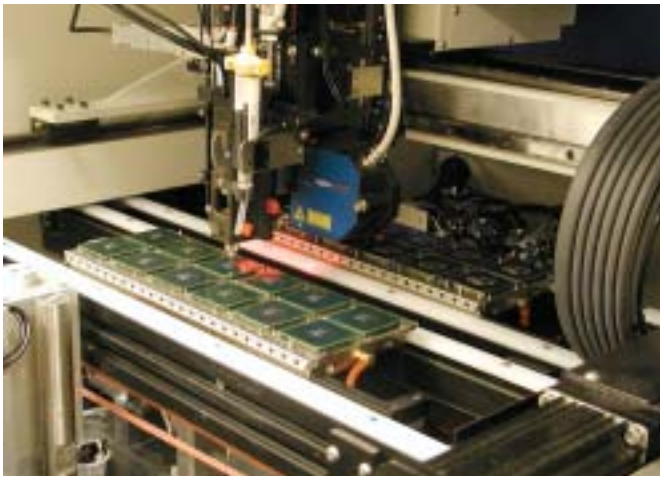

Figure 4. Dual-lane underfill

After the preheated carrier has been indexed into the dispense area, a new carrier is immediately loaded for preheating, ensuring that preheating does not delay the machine.

Dispensing

After preheating, the carrier is indexed to the dispense area and locked in place with vacuum. While in the dispense area, the carrier is heated to speed up the flow of the underfill material. The machine performs vision alignment and height check on each substrate. Vision alignment is performed on the die itself to increase dispense accuracy, since dispensing is done relative to the die edge.

Maintaining the correct offset to the die edge is essential to ensure optimum material flow and has a direct impact on UPH and quality. After alignment, the underfill material is dispensed. Depending on the die size and underfill material, the process may require several passes, usually two to three straight lines of various lengths and one U-shaped pattern.

Pump technology plays a critical role, since dispensing repeatability for small amounts is required in order to ensure a stable quality process in high-volume manufacturing. Rotary or linear positive displacement pumps are often used to dispense underfill material. Many auger pitches, cuts and sizes are used to optimize the process and maximize productivity. Advanced pump technology, mechanical design and flexible software are some of the tools necessary to achieve a high process Cpk.

Substrate Post-heat

After dispense is finished, the carrier is indexed into the post heat area. Post-heating allows the material to finish flowing and allows the air bubbles (voids) to escape, while keeping moisture content low. Having a separate post-heat station increases package reliability and improves system UPH.

Cure Oven

After the underfill dispensing process is finished, the processed carriers are loaded into magazines or transported into a cure oven. Temperatures and dwell times depend on the types of underfill material used and the package size. Once the underfill is cured, the part is a completed, bonded, interconnected packaged system.

Conclusion

The number of applications using flip chip technology will expand rapidly over the next few years. This will drive the demand for next-generation flip chip specific die bonders and underfill dispensers. The combination of flip-chip-technology and these new platforms will provide cost-efficient semiconductor packaging solutions for leading integrated device manufacturers and original and subcontract manufacturers. **AP**

Reference

[1] Miquel, B., "Flip Chip Underfill," Advanced Packaging, Vol. 11, No. 8 (August 2002), p. 33.

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